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10/749,831	12/30/2003	Kevin M. Conley	SNDK.247US0	9380

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EXAMINER	
ELAND, SHAWN	

ART UNIT	PAPER NUMBER
2188	

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12/22/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/749,831	CONLEY ET AL.	
	Examiner	Art Unit	
	SHAWN ELAND	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-4 and 26-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-4 and 26-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09/11/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to the Applicant's response filed on 09/11/08.

Status of Claims

Claims 2 – 4 & 26 – 41 are pending in the Application.

Claims 2 – 3, 28, 31, 36, & 40 have been amended.

Claims 1 & 5 – 25 are cancelled.

Claim 41 is new.

Claims 2 – 4 & 26 – 41 are rejected.

Response to Amendment

Applicant's amendments and arguments filed on 09/11/08 in response to the Office action mailed on 03/19/08 have been fully considered, but they are not persuasive. Therefore, the rejections made in the previous Office action are maintained, and restated below, with changes as needed to address the amendments.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2 – 4 & 26 – 41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 2, 28, 31, 36, & 40 contain the phrase "a minimum number of memory cells" in the preamble of each claim. It is unclear as to how many cells would constitute a minimum number. There is nothing in the Applicant's specification that would define what this means. For the purposes of applying art, the Examiner will assume at least one memory cell would satisfy the minimum number requirement.

The remaining claims are rejected for depending upon the rejected claims above.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 2-4, 28, 29, 31, 32, 34, 36, 38 and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by ***Conley*** (US PG Publication 2002/0099904 A1).

As for claim 2, Conley teaches a method of writing data into a non-volatile memory system of a type having blocks of a minimum number of memory cells that are simultaneously erasable and which individually store a given number of host units of data, comprising:

designating a first of the blocks for storage of a number of units of data with sequential logical addresses that is less than a pre-set proportion of the given number, the pre-set proportion being less than the given number, thereafter responding to a plurality of successive host commands to write a number of units of data less than the pre-set proportion of the given number that have sequential logical addresses by writing their data into a first designated block, and responding to host commands to write a number units of data having sequential logical addresses equal to or in excess of the pre-set proportion of said given proportion of said given number by writing their data into a block other than the first designated block **(paragraph 0062, all lines – the storage capacity of a block is determined as to indicate if the amount of data to be stored is equal to or less than/greater than the capacity of the block. If the capacity is sufficient, the system will try to put the data in a partially written block. If not, the system will address a new block and store the within this block, or across multiple blocks based on the data size – see also Fig. 14. Figs. 8 and 9 further illustrate Conley as physically storing data in a sequential manner (i.e. contiguous pages))**.

To help illustrate this point, assume *arguendo*, that "a number of units of data" (hereinafter given number) is equal to the storage capacity of one of Conley's entire blocks, and that "a pre-set proportion" equals 100% of said given number. Conley's system, determines that a number of writes equal to or greater than said given number could not be written to a partial written block (e.g. first designated block), hence the data would be written to a block other than the first designated block. Also, if the amount of data to be written is less than 100% the capacity of a full block, and there is enough space to write that amount of data to a partially written block, Conley would write that number of units less than 100% of said given number to a

partially written block (e.g. first designated block) in accordance with the flow illustrated in Fig. 14 of Conley.

In regard to claim 28, Conley teaches a method of writing data into a non-volatile memory system of a type having blocks of a minimum number of memory cells that are simultaneously erasable and which individually store a given number of host units of data, comprising:

designating at least a first one of the blocks to store a number of units of data having sequential logical addresses that is less than a pre-set fraction of said given number **(as stated in the rejection of claim 2, the partially written block (as discussed in figure 14) is the first block)**.

thereafter responding to a plurality of successive host commands to individually write units of data into the memory system by determining whether a number of the units of data with sequential logical addresses is less than the pre-set fraction, and, if so, by writing the data into the first designated block, and responding to host commands to write units of data having a number of sequential logical addresses that is equal to or in excess of the pre-set fraction of said given number by writing the data into a block other than the first dedicated block **(paragraph 0062, all lines – the storage capacity of a block is determined as to indicate if the amount of data to be stored is equal to or less than/greater than the capacity of the block. If the capacity is sufficient, the system will try to put the data in a partially written block. If not, the system will address a new block and store the within this block, or across multiple blocks based on the data size – see also Fig. 14. Figs. 8 and 9 further illustrate Conley as physically storing data in a sequential manner (i.e. contiguous pages))**.

To help illustrate this point, assume *arguendo*, that "a number of units of data" is equal to the storage capacity of one of Conley's entire blocks, and that "a pre-set fraction" equals 100% of said given number. Conley's system, determines that a number of writes equal to or greater than said given number could not be written to a partial written block (e.g. first designated block), hence the data would be written to a block other than the first designated block. Also, if the amount of data to be written is less than 100% the capacity of a full block, and there is enough space to write that amount of data to a partially written block, Conley would write that number of units less than 100% of said given number to a partially written block (e.g. first designated block) in accordance with the flow illustrated in Fig. 14 of Conley.

As for claim 31, Conley teaches a method of operating a non-volatile memory system in response to commands received from a host to individually write logically addressed units of data therein, the memory system having memory cells grouped into blocks of a minimum number of memory cells that are simultaneously erasable and which individually store a given number of units of data at individual physical addresses, the logical addresses of received units of data being mapped within the memory system into corresponding physical addresses where the received units of data are stored, comprising:

allocating a first one of the blocks to store units of data having a number of sequential logical addresses less than a fraction of said given number **(Fig. 14, elements 52, 53, 61, 63 – paragraph 0062 – if the system determines that enough space is available to accommodate the amount of data required by the pages corresponding to a number of logical addresses, the data will be allocated to the partially written block),**

allocating a second one of the blocks to store units of data having a number of sequential logical addresses equal to or in excess of the fraction of said given number **(Fig. 14, elements 52, 53, 55 – paragraph 0062 – if the system determines if a sufficient amount of space is not available to accommodate the amount of data required by the pages corresponding to the number of logical addresses, a second block (new erased block) will be allocated to store the data)**,

in response to receipt of a command to write data having a number of sequential logical addresses less than said fraction, determining whether the first block has sufficient erased capacity to store the received data and, if so, writing the received data into sequential physical addresses of the first block **(Fig. 14, elements 61 and 67 – paragraph 0062 – once the system determines that enough pages are available in the partially written block (i.e. element 61), the data will be written into the newly allocated block (element 67))**, and

in response to receipt of a command to write data having a number of sequential logical addresses equal to or in excess of said fraction, determining whether the second block has erased capacity to store the data and, if so, writing the data into sequential physical addresses of the second block **(Fig. 14, elements 55 and 57 – paragraph 0062 – once the system determines that a new erased block is sufficient to store the data, the new data is written to the block (element 57))**.

As for claim 32, Conley teaches,

in response to receipt of the command to write data having a number of sequential logical addresses less than said fraction, if the first block does not have sufficient erased capacity to store the received data, allocating a third one of the blocks to store units of data having a number

of sequential logical addresses less than a fraction of said given number and then writing the received data into sequential physical addresses of the third block **(Fig. 14, elements 65 and 67 – paragraph 0062 – once the system determines that the partial block is not large enough, a new erased block (third) will be allocated and written to)**, and

in response to receipt of the command to write data having a number of sequential logical addresses equal to or in excess of said fraction, if the second block does not have sufficient erased capacity to store the received data, allocating a fourth one of the blocks to store units of data having a number of sequential logical addresses equal to or in excess of the fraction of said given number and then writing the received data into sequential physical addresses of the fourth block **(Fig. 14, elements 55 and 57 – paragraph 0062 – once the system determines that a one new erased block is not sufficient to store the data, an additional block (i.e. fourth) will be allocated to accommodate the new data (elements 55 and 57))**.

As for claim 3, Conley teaches determining whether or not the successive host commands individually include a number of units of data having sequential logical addresses less than the pre-set proportion of said given number **(referring again to paragraph 0062, and the rejections stated above, the given number is based on the size of an entire block)**.

As for claims 4, 29 and 34, Conley teaches the non-volatile memory cells as being organized into multiple sub-arrays, and said blocks of memory cells include memory cells of two or more of the sub-arrays **(paragraph 0062, all lines, if the amount of host data does not exceed the size of one full block the data, two different sets of host writes can be stored uniquely in one block (i.e. each write is a unique sub-array of data within each block). Also**

note Conley specifically teaches his memory system as including sub-arrays in paragraph 0010, lines 1-7).

As for claim 36, Conley teaches a method of writing data into a non-volatile memory system of a type having blocks of a minimum number of memory cells that are simultaneously erasable and which individually store a given number of host units of data, comprising:

designating at least a first one of the blocks to store a number of units of data received by the memory system with individual ones of multiple write commands that have sequential logical addresses less than a pre-set fraction of said given number **(as stated in the rejection of claim 2, the partially written block (as discussed in figure 14) is the first block)**,

responding to the receipt of multiple commands by the memory system to individually write one or more units of data thereinto by, for individual commands **(data is written to the memory in accordance with the host's commands)**,

(a) determining whether the command specifies the writing of a number of units of data having sequential logical addresses that is less than the pre-set fraction **(paragraph 0062, all lines – the system determines the amount of data to write)**, and (b) determining whether the first block has enough erased capacity to store the number of units of data provided with the command **(figure 14, partial blocks are checked to determine if enough capacity is available to store the data before data is either stored in partial block, or to a new one/s)**, wherein

when both of conditions (a) and (b) above are determined to exist, thereafter writing the units of data into the first block **(paragraph 0062, all lines – if less than a**

full block is to be written, and there is enough space in the partially written block, the data will be written to the partially written block), but

when either one of conditions (a) or (b) above is determined not to exist, writing the units of data into one of the blocks other than the first block **(if more data than one the size of one block is to be written or the partial block lacks the capacity to store the entire set of data is written to the new block – figure 14)**.

As for claim 38, Conley teaches:

designating at least a second one of the blocks to store a number of units of data received by the memory system with individual ones of multiple write commands that have sequential logical addresses equal to or greater than the pre-set fraction **(figure 14, element 55, the newly addressed block will store the data)**, and

responding to the receipt of multiple commands by the memory system to individually write one or more units of data thereinto by additionally, for individual commands **(the system will follow the flow illustrated in Fig. 14 for the commands transmitted by the host)**,

(c) determining whether the command specifies the writing of a number of units of data greater than the given number **(Fig. 14, element 53)**, wherein when neither of the conditions (a) nor (c) above exist, writing the units of data into the second block, without regard to whether condition (b) exists or not, but when the condition (c) above is determined to exist, writing the units of data into one of the blocks other than the first or second blocks **(again, (if more data than one the size of one block is to be written or**

the partial block lacks the capacity to store the entire set of data is written to the new block – Fig. 14).

As for claim 40, Conley teaches a non-volatile memory system having memory cells grouped into blocks of a minimum number of memory cells that are simultaneously erasable and which individually store a given number of units of data at individual physical addresses, the logical addresses of received units of data being mapped within the memory system into corresponding physical addresses where the received units of data are stored, a method of operation in response to received commands to individually write logically addressed units of data therein, comprising:

designating a first one of the blocks to store units of data having a number of sequential logical addresses less than a pre-determined fraction of said given number **(as stated in the rejection of claim 2, the partially written block (as discussed in figure 14) is the first block)**,

designating a second one of the blocks to store units of data having a number of sequential logical addresses equal to or in excess of the fraction of said given number **(newly addressed block – Fig. 14, element 55)**,

providing at least another one of the blocks that is fully erased **(Fig. 14, element 57, a block or multiple blocks will be provided depending on the size of the data)**, and

in response to receipt of a command to write data into the memory system, identifying the number of units of the data that have sequential logical addresses, determine whether the number of such units with sequential logical addresses are less than the fraction **(Fig. 14, element 53)**, and, if so,

writing the data to the first of the blocks **(if enough capacity exists in the partially written block, the data will be written in the partial block)**, but if the amount of data is not less than the fraction, then

writing the data to the second of the blocks if there is sufficient capacity therein, but if there is not sufficient capacity in the second of the blocks, writing the data to the fully erased block **(if the partially written block does not have enough space the data will be first written to a newly addressed block, and additional blocks if the additional capacity is required 0 Fig. 14, elements 53, 55, and 57)**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 26, 27, 30, 33, 35, 37, 39, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Conley*** (US PG Publication 2002/0099904 A1) as applied to claims 2 and 28 above, and in further view of ***Kulkarni*** et al. (Us PG Publication 2002/0034105 A1), hereinafter ***Kulkarni***.

As for claims 26, 27, 30, 33, 35, 37, 39 and 41, though Conley teaches all the limitations of claims 2 and 28, he fails to specifically teach the pre-set proportion as being set within a range of 25-75 percent of the given number as recited by Applicant in these claims.

Kulkarni however teaches a system and method for incrementally updating an image in flash memory wherein new flash images are built incrementally until a memory block is of sufficient size to be written to the flash memory – paragraph 0013, all lines. More specifically, Kulkarni teaches writing memory to a first memory block (i.e. RAM), until the memory is half full (i.e. 50 percent), and subsequently writing the data to a second block in the flash memory (i.e. predetermined limit set at 50% allocation) – paragraph 0014, all lines.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Conley to further include Kulkarni's system for updating an image in flash memory into his own system for partial block data programming in a non-volatile memory. By doing so, Conley would have a more efficient memory system capable for reducing the number of sections transmitted during the writing process, while persevering sections that are used to construct other section as taught by Kulkarni in paragraph 0011, all lines. Additionally, Conley could benefit from Kulkarni's system by preventing the problems related to data overwrite as described by Kulkarni in paragraph 0012, all lines.

Response to Arguments

Applicant's arguments filed 09/11/08 have been fully considered but they are not persuasive.

Applicant argues that *a proportion or fraction of a given number do not constitute 100% of that number*. The Examiner respectfully disagrees. A proportion or a fraction may be defined as a small part of something, such as ¼ of element X. But proportion also can be defined as a ratio, such as 1 out of 1, and a fraction as merely one number divided by another, such as 1/1. Both proportion and fraction in the previous examples mean 100% so the Examiner's interpretation still stands. Furthermore, fractions and proportions could also mean more than one, as in 2/1, 3/2, 4/1, etc.

Applicant argues *the Office action ignores that the process occurs for a plurality of units of data "that have sequential logical addresses."* The Examiner has cited in the previous Office action figures 8 & 9 of Conley, showing data physically stored in a sequential manner (i.e. contiguous pages).

Applicant argues *Kulkarni's memory block is not the same as the block defined in the claim language, which is defined as "a minimum number of cells that are simultaneously erasable."* The Examiner points out that the Applicant's further argument that Kulkarni's block is similar to Applicant's page as defined by the instant application (paragraph [0008] of the specification) only proves the Examiner's rejection as correct. Assuming, *arguendo*, that Kulkarni's block really is similar to Applicant's page in which, as defined in paragraph [0008], it takes one or more pages to make up one of Applicant's blocks, then Kulkarni's filling definitely occurs at a proportion of less than 100%. If the page is equal to a block in size, as paragraph [0008] clearly states is possible, then the filling happens at 50% capacity since Kulkarni fills his

memory blocks at 50%. However, if the Kulkarni's blocks, a.k.a. Applicant's pages, are only half the size of Applicant's blocks (i.e. 2 pages per block), then Kulkarni's filling occurs as 25% of the simultaneously erasable block as defined by Applicant. Both of these assumptions fit with the scope of the claims. Further, the specification's paragraph [0008] defines these terms for a "typical flash EEPROM" so in fact it is the Applicant's own admission that it is well known in the art that one or more pages make up a block. In the end, it is Conley that teaches blocks as a minimum number of cells that are simultaneously erasable. It is the combination of Conley and Kulkarni that is used here, not Kulkarni alone. There is nothing in the prior art indicating that it has to take more than two of Kulkarni's blocks to make up the minimum number of cells that are simultaneously erasable, so combining for obviousness is feasible.

Applicant argues *there is no step in figure 14 of Conley that asks whether the incoming data is less than or equal than a pre-set or pre-determined proportion of the given number of units that may be stored in a block*. The Examiner would like to point out that in several of the above claims, different elements of figure 14 were pointed out depending upon the requirements of the claim language above. However, the Examiner would like to point out element 53 in particular indicating whether or not the incoming data is less than or equal to a pre-set proportion of the number of units that may be stored in a block.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Examiner's Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Eland whose telephone number is (571) 270-1029. The examiner can normally be reached on MO - TH, & every other FR.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hyung S. Sough/
Supervisory Patent Examiner, Art Unit 2188
12/19/08

/Shawn Eland/
Examiner, Art Unit 2188
12/22/2008